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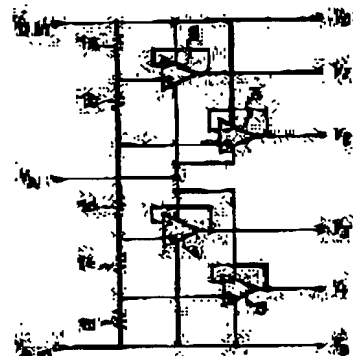
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(54) DRIVING VOLTAGE GENERATING DEVICE FOR LIQUID CRYSTAL DISPLAY DEVICE

(57)Abstract:

PURPOSE: To reduce power consumption to be consumed in a driving voltage generating device.
CONSTITUTION: In a driving voltage generating device for supplying a liquid crystal driving power generating six kinds of voltages V0 to V5 required for driving a liquid crystal display part while dividing an input voltage by voltage dividing resistors 1a to 1e from one kind of liquid crystal driving supply voltage (V0in-V5in), a system power source potential VA to be provided in a liquid crystal display device having the intermediate potential of the liquid crystal driving voltage is used as a power supply in addition to the liquid crystal driving supply voltage.



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[Claim(s)]

[Claim 1] The driver voltage generator of the liquid crystal display which reduced power consumption by applying the electric power supply to the supply voltage for a liquid crystal drive, and doubling and using the system power potential which it has within the liquid crystal display with the in-between potential of the supply voltage for a liquid crystal drive in the driver voltage generator for pressuring input voltage partially, generating six kinds of electrical potential differences required for the drive of the liquid crystal display section, and supplying the power for a liquid crystal drive from one kind of supply voltage for a liquid crystal drive.

[Claim 2] The driver voltage generator of the liquid crystal display which reduced power consumption by applying the electric power supply to the supply voltage for a liquid crystal drive, and using the touch-down potential of the system power electrical potential difference which it has within the liquid crystal display with the in-between potential of the supply voltage for a liquid crystal drive in the driver voltage generator for pressuring input voltage partially, generating six kinds of electrical potential differences required for the drive of the liquid crystal display section, and supplying the power for a liquid crystal drive from one kind of supply voltage for a liquid crystal drive.

[Claim 3] The driver voltage generator of a liquid crystal display according to claim 2 characterized by coming to combine an operational amplifier and a transistor when the potential difference of the output voltage which pressured partially the above-mentioned supply voltage for a liquid crystal drive, and system power potential with the in-between potential of this supply voltage for a liquid crystal drive is small.

[Claim 4] The driver voltage generator of a liquid crystal display according to claim 1 characterized by coming to combine an operational amplifier and a transistor when the potential difference of the output voltage which pressured partially the above-mentioned supply voltage for a liquid crystal drive, and the touch-down potential with the in-between potential of this supply voltage for a liquid crystal drive of system power is small.

[Claim 5] Claim 1 characterized by coming to combine two or more operational amplifiers and transistors when the potential difference of the output voltage which pressured partially the above-mentioned supply voltage for a liquid crystal drive, and system power potential with the in-between potential of this supply voltage for a liquid crystal drive or the touch-down potential of system power is small, and the driver voltage generator of a liquid crystal display according to claim 2.

[Claim 6] The driver voltage generator of a liquid crystal display according to claim 1 characterized by using the potential which carried out the pressure up of the system electrical potential difference when the potential difference with system power potential is smaller than the output voltage which pressured partially the above-mentioned supply voltage for a liquid crystal drive.

[Claim 7] The driver voltage generator of the liquid crystal display according to claim 2 characterized by using the potential which transformed the system electrical potential difference into the negative electrical potential difference when the potential difference with system power potential is smaller than the output voltage which pressured partially the above-mentioned supply voltage for a liquid crystal drive.

[Claim 8] The driver voltage generator of a liquid crystal display according to claim 1 characterized by using the potential which carried out the pressure up of the system electrical potential difference by the booster circuit which used the MOS FET when the potential difference with system power potential is smaller than the output voltage which pressured partially the above-mentioned supply

voltage for a liquid crystal drive.

[Claim 9] The driver voltage generator of a liquid crystal display according to claim 1 characterized by using the potential which transformed the system electrical potential difference into the negative electrical potential difference by the negative electrical potential difference generating circuit which used the MOS FET when the potential difference with system power potential is smaller than the output voltage which pressured partially the above-mentioned supply voltage for a liquid crystal drive.

[Detailed Description of the Invention]

[0001]

[Industrial Application] This invention relates to the driver voltage generator of a liquid crystal display which generates the electrical potential difference for a liquid crystal display panel drive.

[0002]

[Description of the Prior Art] In the conventional simple matrix liquid crystal display (the liquid crystal display of the same drive methods, such as MIM (Metal Insulator Metal), is included), 6 level drive methods which supply the electrical potential difference of six kinds of level to a liquid crystal driver from a driver voltage generator, and drive a liquid crystal display panel are adopted.

[0003] These electrical potential differences use as a power source between 2 electrical potential differences higher (electrical potential difference difference) than the logic power source currently used within a system, and the approach of supplying a partial pressure or the electrical potential difference pressured partially by resistance division to a liquid crystal driver IC through the operational amplifier which made voltage follower connection by resistance division is used. (a detail -- the "Hitachi LCD driver LSI data book" March, 1990 versions P61, P62, and P286 of , Inc. Hitachi, and SANYO Electric [] Co., Ltd. -- "the 1990 Mitsuhiro semi-conductor --"P183 and "LA5311M" edited by data book industrial device integrated-circuit Vol.4 constant voltage power supply explanation [] of P184 -- reference) .

[0004] The example of a circuit which carries out resistance division and generates driver voltage as a conventional circuit of the driver voltage generator of a liquid crystal display using four operational amplifiers 101-104 which made voltage follower connection in five resistance 100a-100d in drawing 20 is shown. It is an electrical potential difference required for the liquid crystal drive supplied from the outside V0inch and V5inch in this drawing 20 . Pressure partially by Resistance 100a-100d based on this, and four kinds of electrical potential differences are made. The electrical potential differences V1, V2, V3, and V4 low-impedance-ized with four operational amplifiers 101-104 which made voltage follower connection are made, six kinds of potentials which applied the electrical potential differences V0 and V5 which are the potentials currently supplied from the outside are generated, and the liquid crystal display is supplied. In addition, although V0 electrical potential difference and V5 electrical potential difference may also be generated with an operational amplifier using an electrical potential difference lower than an electrical potential difference higher than V0 electrical potential difference and V5 electrical potential difference, since the circuit shown by drawing 20 is a minimum configuration, explanation is omitted. In addition, all the operational amplifiers used as a voltage follower are using between the above-mentioned electrical potential differences by which resistance division is carried out as power-source potential and touch-down potential. Moreover, the technique of reducing the output capacity of an operational amplifier and reducing the consumed electric current of the operational amplifier itself is also proposed by JP,5-313612,A.

[0005] Hereafter, before explaining a circuit to a detail conventionally [above-mentioned], the current in a liquid crystal panel is explained to an example for the case where a liquid crystal display as first shown by drawing 16 is driven. In drawing 16 , the liquid crystal panel 52 consists of common electrodes of n segment electrodes [53 or m] which sandwiched the liquid crystal ingredient, and the segment driver 55 which can carry out the selection switch of the electrical potential difference of electrical potential differences V0, V2, V3, and V5 is connected to the segment electrode 53. Moreover, the common driver 56 which can carry out the selection switch of the electrical potential difference of V0, V1, V4, and V5 is connected to the common electrode 56. Furthermore, the electrical potential difference of 6 level of electrical potential differences V0, V1, V2, V3, V4, and V5 is supplied to the segment driver 55 and the common driver 56 by the driver voltage generator 51. In addition, the driver voltage generator 51 shall be constituted by the circuit shown by drawing 19 .

[0006] The liquid crystal drive wave in the common electrode 54 of the liquid crystal panel 52 shown in above-mentioned drawing 16 and the electrode of the arbitration of the segment electrode 53 has become like the segment output wave of drawing 18 like the common output wave of drawing 17 at the segment side at the common side. As for drawing 18 (a), liquid crystal shows the drive wave at the time of repeating lighting and an astigmatism LGT to the line writing direction for drawing 18 (c) among this drawing 18 at the time of liquid crystal complete lighting at the time of a liquid crystal astigmatism LGT, as for drawing 18 (b).

[0007] Based on above-mentioned drawing 18, the direction of the current which flows within the liquid crystal of the liquid crystal display panel 52 was analyzed, and drawing 19 illustrated the outline. As for drawing 19 (a), liquid crystal shows the direction of the current in liquid crystal at the time of repeating lighting and an astigmatism LGT to the line writing direction for drawing 19 (c) among drawing 19 like above-mentioned drawing 18 at the time of liquid crystal complete lighting at the time of a liquid crystal astigmatism LGT, as for drawing 19 (b).

[0008] As above-mentioned drawing 19 shows, drawing 19 (a) is the case where drawing 19 (c) repeats lighting and an astigmatism LGT to a line writing direction at the time of complete lighting in drawing 19 (b) at the time of a liquid crystal astigmatism LGT. The current in a liquid crystal display also has the current which is not flowing among V_{supply} maximum electrical-potential-difference V_{0-5} , for example, not necessarily flows between V_{V0-2} or between V_{V3-5} like current I^{**} of drawing 19 (c) so that drawing 19 may be seen and understood. Especially this current I^{**} will become large indeed, if the repeat of lighting of the direction of a liquid crystal display train and an astigmatism LGT increases, and there are also very many ratios to the whole. To it, the current shown by current I^{**} or current $I^{**'}$ and current I^{***} is a current accompanying the line selection pulse of a common output, and a current value is seldom influenced with the display screen.

[0009] In the driver voltage generator of the liquid crystal panel which takes the above current paths, drawing 20 illustrated the motion of the current inside an electrical-potential-difference generator supposing the load model corresponding to the current shown in current I^{**} of drawing 19 (c) in a circuit conventionally shown in drawing 20.

[0010] The model load in above-mentioned drawing 20 connects at a serial the load 107 and switching circuit 109 which have the impedance of Z_L among V_{V0-2} , and inserts in a serial the load 108 and switching circuit 110 which have the impedance of Z_L' among V_{V3-4} . Switching circuits 109 and 110 correspond here, when corresponded to alternating current-ization at the time of a liquid crystal drive, and a switching circuit 109 closes an alternating current-ized (+) period, a switching circuit 110 opens it, a switching circuit 109 opens an alternating current-ized (-) period and the switching circuit 110 has closed, and there is nothing that switching circuits 109 and 110 close to coincidence (it opens), and the rate of closing motion is [every / 2 / 1].

[0011] The current of each part when a switching circuit 109 closes and the switching circuit 110 is open is expressed with the arrow head of a continuous line to above-mentioned drawing 20, and the current when a switching circuit 109 opens and the switching circuit 110 has closed is expressed with the arrow head of a broken line. Here, each self-consumed electric current of an operational amplifier 101, 102, 103, 104 is the average consumed electric current of the whole circuit, if it is I_{s1} , I_{s2} , I_{s3} , and I_{s4} and the current which flows the current which flows for a load 107 for I_z and a load 108 is made into I_z' . $I_{s1}+I_{s2}+I_{s3}+I_{s4}+(I_z+I_z')/2 \cdots (1)$

It is come out and expressed.

[0012] However, although $I_{s1}=I_{s2}=I_{s3}=I_{s4}$ and $I_z=I_z'$ are not satisfied completely, therefore the potential amendment circuit is prepared, also when it may become 5% of all currents, and about 10% of numbers depending on a liquid crystal display system and effectiveness is seldom acquired in the case of such a system, it generates.

[0013]

[Problem(s) to be Solved by the Invention] The current to which an operational amplifier flows to bleeder resistance like before as compared with the configuration which only divides an electrical potential difference by resistance, and obtains it with the configuration by which voltage follower connection is made can be reduced sharply, and the precision of output voltage can be improved. However, the conventional configuration has caused increase of the consumed electric current for the following reasons.

[0014] Current supply to an operational amplifier is performed by maximum

electrical-potential-difference terminal V0inch supplied from the outside, and V5inch conventionally [above-mentioned] in the circuit. Since the difference of this electrical potential difference and the output terminal electrical potential differences V1-V4 is large, this electrical-potential-difference difference is consumed as heat within the operational amplifier which is operating as a series regulator. For example, since the power which a current is supplied and is expressed with the product of the electrical potential difference between VV0-3 which are the electrical-potential-difference difference, and the supply current of V3 serves as heat from V0 and it will be consumed within an operational amplifier when supplying a current from V3 terminal, effectiveness is very bad.

[0015]

[Means for Solving the Problem]

(The 1st means) the driver voltage generator for pressuring input voltage partially, generating six kinds of electrical potential differences required for the drive of the liquid crystal display section, and supplying the power for a liquid crystal drive from one kind of supply voltage for a liquid crystal drive, -- setting -- the electric power supply -- the supply voltage for a liquid crystal drive -- in addition, power consumption is reduced by doubling and using the system power potential which it has within the liquid crystal display with the in-between potential of the supply voltage for a liquid crystal drive.

[0016] (The 2nd means) the driver voltage generator for pressuring input voltage partially, generating six kinds of electrical potential differences required for the drive of the liquid crystal display section, and supplying the power for a liquid crystal drive from one kind of supply voltage for a liquid crystal drive, -- setting -- the electrical-potential-difference supply -- the supply voltage for a liquid-crystal drive -- in addition, power consumption is reduced by using the touch-down potential of the system power electrical potential difference which it has within the liquid crystal display with the in-between potential of the supply voltage for a liquid crystal drive.

[0017] (The 3rd means) When the potential difference of the output voltage which pressured partially the above-mentioned supply voltage for a liquid crystal drive, and system power potential with the in-between potential of the supply voltage for a liquid crystal drive is small, it has the 2nd means realized combining the operational amplifier and the transistor.

[0018] (The 4th means) When the potential difference of the output voltage which pressured partially the above-mentioned supply voltage for a liquid crystal drive, and the touch-down potential with the in-between potential of the supply voltage for a liquid crystal drive of system power is small, it has the 1st means of the above realized combining the operational amplifier and the transistor.

[0019] (The 5th means) When the potential difference of the output voltage which pressured partially the above-mentioned supply voltage for a liquid crystal drive, and system power potential with the in-between potential of the supply voltage for a liquid crystal drive or the touch-down potential of system power is small, it has the 1st means of the above and the 2nd means which were realized combining an operational amplifier and a transistor two or more.

[0020] (The 6th means) When the potential difference with system power potential is smaller than the output voltage which pressured partially the above-mentioned supply voltage for a liquid crystal drive, it has the 1st means of the above realized using the potential which carried out the pressure up of the system electrical potential difference.

[0021] (The 7th means) When the potential difference with system power potential is smaller than the output voltage which pressured partially the above-mentioned supply voltage for a liquid crystal drive, it has the 2nd means of the above realized using the potential which transformed the system electrical potential difference into the negative electrical potential difference.

[0022] (The 8th means) When the potential difference with system power potential is smaller than the output voltage which pressured partially the above-mentioned supply voltage for a liquid crystal drive, it has the 1st means of the above realized using the potential which carried out the pressure up of the system electrical potential difference by the booster circuit which used the MOS FET.

[0023] (The 9th means) When the potential difference with system power potential is smaller than the output voltage which pressured partially the supply voltage for a liquid crystal drive, it has the 1st means realized using the potential which transformed the system electrical potential difference into the negative electrical potential difference by the negative electrical-potential-difference

generating circuit which used the MOS FET.

[0024]

[Function]

(Operation of the 1st means) according to the 1st means -- the drive power for liquid crystal -- the above-mentioned former -- a circuit -- receiving -- about -- it can decrease now to one half. Moreover, since they can lower pressure-proofing of use components while reduction of required components mark is attained to the conventionally same components mark as a circuit, the cost of them can be cut down. That is, a cheap liquid crystal display is realizable by using the driver voltage generating circuit of this configuration with a low power.

[0025] (Operation of the 2nd means) according to the 2nd means -- the drive power for liquid crystal -- the above-mentioned former -- a circuit -- receiving -- about -- it can decrease now to one half. Moreover, since they can lower pressure-proofing of use components while reduction of required components mark is attained to the conventionally same components mark as a circuit, the cost of them can be cut down. That is, a cheap liquid crystal display is realizable by using the driver voltage generating circuit of this configuration with a low power.

[0026] (Operation of the 3rd means) The configuration in the 2nd means of the above can make it possible to acquire an operation equivalent to the 2nd means also in a difficult system according to the 3rd means only by adding one transistor. [0027] (Operation of the 4th means) The configuration in the 1st means can make it possible to acquire an operation equivalent to the 1st means also in a difficult system according to the 4th means only by adding one transistor.

[0028] (Operation of the 5th means) The configuration in the 1st means and 2nd means can make it possible to acquire an operation equivalent to the 1st means and the 2nd means by the addition of two transistors also in a difficult system according to the 5th means.

[0029] (Operation of the 6th means) According to the 6th means, also in the display system which was not able to apply the configuration of the 1st means, by using a booster circuit shows that the configuration of the 1st means is realizable. Thereby, even if it is the liquid crystal display of what kind of system electrical potential difference, an operation of the 1st means can be acquired.

[0030] (Operation of the 7th means) According to the 7th means, also in the display system which was not able to apply the configuration of the 2nd means, by using a negative electrical-potential-difference generating circuit shows that the configuration of the 2nd means is realizable. Thereby, even if it is the liquid crystal display of what kind of system electrical potential difference, an operation of the 2nd means can be acquired.

[0031] (Operation of the 8th means) According to the configuration of the booster circuit using the MOS FET by the 8th means, a booster circuit with very sufficient power efficiency can be created. That is, the power circuit for a liquid crystal drive and liquid crystal display which are shown in the 6th means can consist of low powers by using this booster circuit.

[0032] (Operation of the 9th means) According to the configuration of the negative electrical-potential-difference generating circuit using the MOS FET by the 9th means, a negative electrical-potential-difference generating circuit with very sufficient power efficiency can be created. That is, the power circuit for a liquid crystal drive and liquid crystal display which are shown in the 7th means can consist of low powers by using this negative electrical-potential-difference generating circuit.

[0033]

[Example]

(Example 1) The example of the driver voltage generator of the liquid crystal display by this invention is shown in drawing 1. To the liquid crystal display panel 52 by which the basic configuration of a liquid crystal display in this example sandwiched the liquid crystal ingredient between the segment electrode 53 and the common electrode 54 as shown in drawing 16, the segment driver 55 and the common driver 56 are connected, and the driver voltage generator 51 is connected to the segment driver 55 and the common driver 56. This configuration does not need to be the components which not necessarily became independent, and also when driver voltage generator 51 the very thing is accumulated by one component, it is included in the segment driver 55 and common driver 56 pan.

[0034] First, on the occasion of a basic configuration, the above-mentioned driver voltage generator 51 which is a driver voltage generator of the liquid crystal display of this invention is described. this driver voltage generator 51 -- drawing 1 -- like -- the maximum electrical potential differences V0

and V5 for a drive -- a power source input (V0 -- high pressure --) Resistance of 1a, 1b, 1c, 1d, and 1e which make V5 low voltage and pressure this electrical potential difference partially on four kinds of electrical potential differences, V1', V2', V3', and V4'. It has the operational amplifiers 2, 3, 4, and 5 which can output the electrical potential difference of V1, V2, V3, and V4 by low impedance by making into reference voltage the electrical potential difference in which the partial pressure was carried out by the resistance.

[0035] The above-mentioned operational amplifier is possible also for V1, V2, V3, the current supply source to V4 output, and current suction from an output terminal, and it operates as a series regulator which constant-voltage-ized the current from + power supply terminal in the case of the current supply source, in current absorption, a current is emitted from an output terminal to - power supply terminal, and it serves to keep output voltage constant.

[0036] Moreover, - power supply terminal of operational amplifiers 2 and 3 and + power supply terminal of operational amplifiers 4 and 5 are connected to system power VA which has the middle potential between V0 and V5 further. Potential of VA is made into $V2 > VA > V3$ here.

[0037] On the other hand, generally V0 inch and VA on the basis of two kinds of power-system V5 electrical potential differences supplied here are supplied by the system power circuit shown in drawing 2. In drawing 2, VS efficiently constant-voltage-ized by the DC to DC converter circuit 7 from the direct-current-voltage source of supply 6 of potential VB is created, and the still higher electrical potential difference VEE is further created by the DC to DC converter circuit 8 from VS. In addition, although capacitor 7a shown with a broken line is a capacitor built in in the DC to DC converter circuit 7, it is daring illustrate it.

[0038] As V0, VA, and V5 which are shown within relation top 0 of correlation with drawing 1, the supply voltage output of the system power circuit shown in above-mentioned drawing 2 is explained below, although generally written like +VEE, and VS and GND. That is, to drawing 1, electrical-potential-difference supply of VA-V5 will be set to V0-V5.

[0039] Here, the cell shown as a notation by a diagram is sufficient as the direct-current-voltage source of supply 6 shown in drawing 2, and what exchanged the commercial alternating current power source for the direct current is replaced. Moreover, although DC to DC converter 7 converts the power efficiently to direct current voltage which is different from a direct-current-voltage source of supply and it is a series regulator, a switching regulator, etc., for a certain reason, it may also be the system of the form, i.e., the power-source configuration of VS=VB, where DC to DC converter 7 was omitted to use the direct-current-voltage source of supply 6 as it is depending on a system. Furthermore, the input of DC to DC converter 8 which outputs +VEE electrical potential difference in drawing 2 is also the same as when you may connect with the direct-current-voltage source of supply 6 and it completely supplies from the direct-current-voltage feeder of another network, although it has connected with VS terminal.

[0040] Here, as the above-mentioned conventional technique showed, drawing 4 assumed the model load equivalent to the load in a liquid crystal panel. In drawing 4, 10 and 11 show the load model. The load 10 is connected to the switching circuit 12 and the serial among VV0-2, and among VV3-5, a load 11 is made into a switching circuit 13 and a serial, and is connected.

[0041] Here, switching circuits 12 and 13 correspond, when corresponded to alternating current-ization of a liquid crystal panel drive, and a switching circuit 12 closes an alternating current-ized (+) period, and a switching circuit 13 opens it, and a switching circuit 12 opens an alternating current-ized (-) period and the switching circuit 13 has closed. In addition, in order to prevent direct current voltage remaining to a liquid crystal panel, the closing motion rate of the switching circuits 12 and 13 in a fixed period is set to one half from being controlled so that an alternating current-ized (+) period and an alternating current-ized (-) period become equal, respectively.

[0042] Furthermore, in drawing 4, a switching circuit 12 closes, and the arrow head of a continuous line shows the current of each part when the switching circuit 13 is open, and the arrow head of a broken line shows the current when a switching circuit 12 opens and the switching circuit 13 has closed.

[0043] Here, each self-consumed electric current of operational amplifiers 2, 3, 4, and 5 is IS1, IS2, IS3, and IS4, and the current to which the current which flows for a load 10 flows for IZ and a load 11 is IZ'. When the switching circuit 12 has closed (the switching circuit 13 is opened), the current shown as the continuous line of drawing 4 flows. That is, the current which the current which flows

into the A point of drawing is $(IS1+IS2+IZ)$, and flows out from an A point is the difference $(IS1+IS2+IZ)$ of this current, although set to $(IS3+IS4)$. - $(IS3+IS4)$

It will flow outside from a ** VA terminal.

[0044] Moreover, when the switching circuit 13 has closed (the switching circuit 12 is opened), the current shown by the broken-line arrow head of drawing flows. It is - $(IS1+IS2)$ in this case $(IS3+IS4+IZ')$ like the above-mentioned case.

It will be supplied from a ** VA terminal.

[0045] namely, the case where a current will flow out outside from VA terminal of drawing 1 if it thinks together with drawing 2 -- system power VS (VA) -- when it will be returned again and a current flows in from VA terminal, it will be again supplied from the system current VS (VA).

Namely, power in the whole power circuit $(V0-V5) \times (IS1+IS2+IZ/2)$

- $1/2 \times (VA-V5) \times \{(IS1+IS2+IZ) - (IS3+IS4)\}$

+ $1/2 \times (VA-V5) \times \{(IS3+IS4+IZ') - (IS1+IS2)\}$

= $V0-V5 \times (IS1+IS2+IZ/2)$

- $VA-V5 \times \{(IS1+IS2+IZ/2) - (IS3+IS4+IZ'/2)\} = (V0-V5) \times (IS1+IS2+IZ/2) + (VA-V5) \times (IS3+IS4+IZ'/2) --$
(2)

It is expressed by carrying out.

[0046] When this sets to $(IS1+IS2+IZ/2) - (IS3+IS4+IZ'/2) = X$ and the balance of the time of $X = 0$, i.e., a load, is equal $(V0-V5) \times (IS1+IS2+IZ/2) --$ (3)

It can express by carrying out. Moreover, the balance of a load differs, when set to $X > 0$, it sets, and it is circuit power. $(V0-V5) \times (IS1+IS2+IZ/2) - (VA-V5) \times X --$ (4)

Furthermore, when set to $X < 0$, it sets. $(V0-V5) \times (IS3+IS4+IZ'/2) - (V0-V5) \times X --$ (5)

It can express by carrying out.

[0047] In addition, they will open and close the short period to the pan corresponding to an indicative data, and in explanation of drawing 4, although explained as opening and closing by turns, if switching circuits 12 and 13 model a liquid crystal display still more strictly, they will express the average current as IZ and IZ' also in the period explained that the switching circuit has closed switching circuits 12 and 13 as shown in drawing 5.

[0048] The current by closing motion of the switching circuit in these short periods will appear in VA terminal as momentary charge and the discharge current, although liquid crystal is a capacitive load therefore. Therefore, since these currents appear as a ripple voltage of VA terminal, i.e., system power VS, capacitor 7a shown in drawing 2 is needed. Although the value of the electrostatic capacity C of capacitor 7a needs to ask for peak voltage by the time constant circuit which includes the output resistance of the electrode resistance in a liquid crystal panel, a segment driver, and a common driver, the equivalence internal resistance of a liquid crystal driver voltage generating circuit, etc. strictly, the electrostatic capacity C in the worst conditions which disregarded these elements in estimate is computable with a bottom type. Namely, electrostatic capacity C of capacitor 7a $C = CLCD \times (V0-V2) / \Delta V --$ (6)

It can express by carrying out.

[0049] Here, ΔV and CLCD are the segment electrode of a liquid crystal panel about the permission ripple voltage of system power. - It is common inter-electrode electrostatic capacity. As an example, by the 640x480 dot matrix LCD, driver voltage 26V between VV0-5, The specific inductive capacity of 0.3x0.3mm, inter-electrode gap 6micrometer, and liquid crystal at the time of 10 and an astigmatism LGT at the time of lighting in the liquid crystal display in 4 [for the bias ratios 1/13, commonness, and segment electrode width of face] $CLCD = (4+10) / 2 \times 10^{-9} / (36 \times \pi) \times 640 \times 480 \times (0.3 \times 10^{-3})^2 / (6 \times 10^{-6}) = 0.285 \times 10^{-6} [F] = 0.285 [\mu F]$

$V0-V2 = 26 \times 2 / 13 = 4 [V]$

Come out, and it is and is a ripple voltage. If it is going to hold down to $\Delta V = 100mV$ $C = 0.285 [\mu F] \times 4 / 0.1 = 11.4 [\mu F]$

It is computable by carrying out.

[0050] The capacitor of a bigger value than this electrostatic capacity is being used for the common output capacitor of a DC to DC converter, and it is not necessary to add capacitor 7a shown by drawing 1 to this inventions, and means that the capacitor conventionally used for the DC to DC converter can be diverted as it is.

[0051] (Example 2) Not only the circuitry that shows the configuration of the system power circuit of this equipment to drawing 2 but in a system power circuit as shown in drawing 3, it thinks. In

drawing 3 , VS efficiently constant-voltage-ized by the DC to DC converter circuit 7 from the direct-current-voltage source of supply 6 of potential VB is created, and electrical-potential-difference(-) VEE lower than system touch-down potential (GND) is further created by the DC to DC converter circuit 9 from VS. In addition, although capacitor 7a shown with a broken line is a capacitor built in in the DC to DC converter circuit 7, it is daring illustrate it.

[0052] Here, the cell shown as a notation by a diagram is sufficient as the direct-current-voltage source of supply 6 shown in drawing 3 , and what changed the commercial alternating current power source into the direct current is replaced. Moreover, although DC to DC converter 7 converts the power efficiently to direct current voltage which is different from a direct-current-voltage source of supply and it is a series regulator, a switching regulator, etc., for a certain reason, it may also be the system of the form, i.e., the power-source configuration of $VS=VB$, where DC to DC converter 7 was omitted to use the direct-current-voltage source of supply 6 as it is depending on a system. Furthermore, the input of DC to DC converter 9 which outputs -VEE electrical potential difference in drawing 3 is also the same as when you may connect with the direct-current-voltage source of supply 6 and it completely supplies from the direct-current-voltage feeder of another network, although it has connected with VS terminal.

[0053] Generally the supply voltage output of drawing 3 is written like VS, GND, and -VEE. If such supply voltage is made to correspond to V0, VA, and V5 of drawing 1 , respectively, the completely same actuation as the case of an example 1 can be performed only by it being different that two kinds of power sources are supplied between V0 inch-V5inch and V0 inch-VA. The power consumption of a driver voltage generating circuit becomes what was shown by the above-mentioned (1) formula, and can acquire the same effectiveness as the case of an example 1. However, it must be electrical-potential-difference $VS(V0) > V2 > GND (VA)$.

[0054] (Example 3) The electrical-potential-difference range which it can output to an operational amplifier that the electrical potential difference exceeding the supply voltage of an operational amplifier cannot be outputted as an own property of an operational amplifier from the first becomes still narrower than a power range. When + power supply terminal electrical potential difference of an operational amplifier is [V+ and - power supply terminal electrical potential difference] generally V-, the maximum of output voltage in case an operational amplifier supplies a fixed current can show the minimum value of operational amplifier output voltage in case $V+\text{-}\Delta V_H$ and an operational amplifier input a fixed current in the form of $V+\text{-}\Delta V_L$. since [therefore,] the intermediate voltage VA in the circuit shown in drawing 1 is used as + supply voltage and - supply voltage of an operational amplifier as examples 1 and 2 -- $VA\text{-}\Delta V_H > V3$ and -- $VA+\Delta V_L < V2$ -- namely, -- It is necessary to fulfill the conditions of $V3+\Delta V_H < VA < V2\text{-}\Delta V_L$.

[0055] In the operational amplifier which consisted of BAIPORA, since ΔV_H and ΔV_L generally serve as about 1v and a comparatively large value, also when application is difficult, it thinks with the circuit of drawing 1 . For example, in LM64P10 which are the liquid crystal unit of our company, it is the specification of minimum electrical-potential-difference difference 4.75V between V0-V5 maximum electrical-potential-difference difference =26.7V and V0-VAs on the assumption that a system power circuit as shown in drawing 3 , and a bias ratio is 1/13.

[0056] In this case, since it becomes impossible for the electrical-potential-difference difference between V2-VAs to take only $4.75V\text{-}(26.7V / 13 \times 2) = 0.64V$, it is difficult the difference to use the operational amplifier which remained as it was and consisted of BAIPORA of a low price in the circuit of drawing 1 .

[0057] Having such made application possible also in conditions is the circuit shown in drawing 6 . In drawing 6 , the output of an operational amplifier is further connected to the base of PNP transistor 3a using the operational amplifier which used V0 and V5 as + power source and - power source as an object for V2 voltage outputs, and the collector of transistor 3a serves as V2 output while connecting with VA and connecting the emitter of transistor 3a to - volt input of an operational amplifier 3. In the case of this circuit, it works so that V2 level may be stabilized, and the output voltage of an operational amplifier 3 takes the electrical-potential-difference value of V2-VBE (the base emitter electrical potential difference of a transistor is set to VBE). When the rate of direct current amplification of a transistor is set to hFE and the suction current of V2 output terminal is I2, the current of $I2/hFE$ flows in the base of a transistor, and the current of $I2(1-1/hFE)$ which is remaining most is supplied to it as collector current of a transistor to VA terminal.

[0058] The electrical-potential-difference difference demanded between V2 and VAs in this case will

be low made to collector-saturation-voltage $V_{CE(sat)}$. namely, the relation of $V_2 - V_{CE(sat)} > V_A$ -- it is -- ****ing -- ***** -- $V_{CE(sat)}$ -- about 0.2 -- it is about V . Therefore, when the electrical-potential-difference difference of a system electrical potential difference and the liquid crystal supply voltage V_2 is extremely small, power consumption can be effectively reduced using this circuit.

[0059] In addition, since V_0 - V_5 are used as a power source of an operational amplifier 3 when this circuit is used, Although the power of $x(V_A - V_5)$ ($I_S + I_2/hFE$) will increase to the circuit of drawing 1 when the consumed electric current I_S and base current I_2/hFE at the time of no-load [an operational amplifier's / own] flow Base current can be reduced when hFE uses a to some extent big transistor, Moreover, since current absorption capacity can also make it a small operational amplifier (I_S is generally also small) compared with the case where direct current absorption is performed, with an operational amplifier, power of this part can fully be made very small.

[0060] Moreover, in drawing 6, while being able to acquire the same effectiveness even if it uses the field-effect transistor of metal-oxide-semiconductor structure although the case where it constitutes using the transistor of BAIPORA is shown, the electrical potential difference equivalent to $V_{CE(sat)}$ as used in the field of a transistor, i.e., the electrical potential difference expressed with the on resistance between the drain-sources of a field-effect transistor and the product of the load current, may be made still smaller than a bipolar transistor.

[0061] (Example 4) On the other hand, in drawing 1, although the relation of the electrical potential difference of V_A and V_3 is $V_A > V_3$, an example when the electrical-potential-difference difference is very small is shown in drawing 7. In drawing 7, the output of an operational amplifier is further connected to the base of NPN transistor 4a using the operational amplifier 4 which used V_0 and V_5 as + power source and - power source as an object for V_3 voltage outputs, and the collector of transistor 4a serves as V_3 output while connecting with V_A and connecting the emitter of transistor 4a to - volt input of an operational amplifier 4. In the case of this circuit, it works so that V_3 level may be stabilized, and the output voltage of an operational amplifier 4 takes the electrical-potential-difference value of $V_3 + V_{BE}$. Here, it is the base-emitter electrical potential difference of a transistor. When the rate of direct current amplification of a transistor is set to hFE and the supply current from V_3 output terminal is I_3 , the current of I_3/hFE flows in the base of transistor 4a, and the current of $I_3(1-1/hFE)$ which is remaining most is supplied to it from V_A terminal as collector current of a transistor.

[0062] An electrical-potential-difference difference required for V_A and V_3 in this case is to be able to do low to collector-saturation-voltage $V_{CE(sat)}$. That is, what is necessary is just the relation of $V_3 + V_{CE(sat)} < V_A$, and $V_{CE(sat)}$ is stopped by less than [0.2V]. In addition, since V_0 - V_5 are used as a power source of an operational amplifier 4 like the above-mentioned example 3 when this circuit is used, Although the power of $x(V_0 - V_A)$ ($I_S + I_2/hFE$) will increase to the circuit of drawing 1 when the consumed electric current I_S and base current I_2/hFE at the time of no-load [an operational amplifier's / own] flow Base current can be reduced when hFE uses a to some extent big transistor, Moreover, since current absorption capacity can also make it a small operational amplifier (I_S is generally also small) compared with the case where direct current absorption is performed, with an operational amplifier, power of this part can fully be made very small. Moreover, a transistor may use a field-effect transistor (FET).

[0063] (Example 5) What is necessary is just to take a configuration like drawing 8 which combined the example 3 and the example 4 complexly, in using further the system electrical potential difference which has V_A level with which can be satisfied of neither $V_3 + \Delta V_H < V_A$ nor $V_A < V_2 - \Delta V_L$, although it is electrical-potential-difference $V_3 < V_A < V_2$.

[0064] In drawing 8, the output of an operational amplifier 3 is further connected to the base of PNP transistor 3a using the operational amplifier 3 which used V_0 and V_5 as + power source and - power source as an object for V_2 voltage outputs, and the collector of a transistor 3 serves as V_2 output while connecting with V_A and connecting the emitter of a transistor 3 to - volt input of operational amplifier 3a. Moreover, the output of an operational amplifier 4 is further connected to the base of NPN transistor 4a using the operational amplifier 4 which used V_0 and V_5 as + power source and - power source as an object for V_3 voltage outputs, and the collector of a transistor 4 serves as V_3 output while connecting with V_A and connecting the emitter of a transistor 4 to - volt input of operational amplifier 4a.

[0065] Relation of V_2 , V_A , and V_3 to the circuit shown in drawing 8 although it is as the example 3

and the example 4 having explained actuation $V_3 + V_{CE}(\text{transistor } 4a) < V_A < V_2 - V_{CE}(\text{transistor } 3a)$. In the case of a next door and a very low electrical-potential-difference difference, it becomes utilizable.

[0066] (Example 6) When becoming electrical-potential-difference $V_A < V_3$, in the circuitry of this invention, application as it is is difficult. Also in this case, as an applicable example, the example in the case of the configuration of the system power circuit shown in drawing 2 is shown in drawing 9. Drawing 9 adds the electrical-potential-difference booster circuit 14 which generates VS' ($VS' > VS$) by making between VS -GND into supply voltage to drawing 2.

[0067] Hereafter, if the pressure up of the electrical potential difference VS is doubled, a detail will be explained about the system in the case of the ability to do more highly than the above-mentioned V_3 (though natural, when $V_3 < 2 \times VS = VS' < V_2$ can be satisfied). As a booster circuit in this case, if it is made the configuration of drawing 11, generating of an electrical potential difference is very efficiently possible. 16 and 17 are equipped with the capacitors 18 and 19 as a transfer switch and a charge storage means in drawing 11.

[0068] The transfer switch 16 is equipped with fixed-end child 16a connected to the input terminal VS , fixed-end child 16b connected to output terminal VS' , and switch terminal 16c which switches connection with a capacitor 18 to either of the fixed-end children 16a and 16b. Moreover, the transfer switch 17 is equipped with fixed-end child 17a connected to the input terminal GND, fixed-end child 17b connected to output terminal VS' , and switch terminal 17c which switches connection with a capacitor 18 to either of the fixed-end children 17a and 17b.

[0069] Moreover, a capacitor 18 stores temporarily the electrical potential difference supplied between VS -GND, i.e., a charge, an end is connected with switch terminal 16c of said transfer switch 16, and the other end is connected to fixed-end child 17c of a transfer switch 17. Transfer switches 16 and 17 are controlled to switch to coincidence in this direction for these transfer switches to connect between [16a and 16c] fixed time amount, and 17a and 17c, and to connect between [16b and 16c] following fixed time amount, and 17b and 17c.

[0070] Actuation in the above-mentioned circuit can be explained as follows.

** Supposing transfer switches 16 and 17 have switched in the direction shown as the continuous line of this drawing first, a capacitor 18 will charge at the electrical potential difference of (VS -GND).

** If transfer switches 16 and 17 switch in the direction shown with the broken line of drawing on the other hand, the charge of an amount according to the capacity factor of capacitors 18 and 19 will be accumulated to a capacitor 19.

[0071] Here, by C, by repeating actuation of ** and **, the charge accumulated in a capacitor 19 will become $Q = C_x (VS - GND) (1/2 + 1/4 + 1/8 + 1/16 + \dots)$, and both the electrostatic capacity of capacitors 18 and 19 will converge the electrical potential difference between terminals of a capacitor 19 on (VS -GND), supposing the charge of a capacitor 19 is 0. Here, since the negative electrode of a capacitor 19 is connected to the input terminal VS , output terminal VS' will generate the potential of $2 \times (VS - GND)$.

[0072] When a load is connected to VS' and the connect time by the side of a of transfer switches 16 and 17 and b supplies the fixed current I by one half in repeat frequency [of a switch switch] f [Hz], respectively, output voltage variation (ripple voltage) ΔV of VS' is expressed with a bottom type. $\Delta V = 3 \times I / (2 \times C \times f)$

It comes out, and it is and the frequency of transfer switches 16 and 17 and the capacity of capacitors 18 and 19 can be set up based on the required load current and a required ripple voltage.

[0073] Moreover, the current supplied from VS terminal is set to $2 \times I$.

[0074] Furthermore, the features of this power circuit are that not only supply of a charge but a charge can be absorbed from VS' , and it can return it to VS . Namely, the charges with which a charge is accumulated in an inflow (a current flows in) and a capacitor 19 to VS' terminal increase in number more than $C_x (VS - GND)$, and Q is electrical-potential-difference [of a capacitor 19] between terminals $> (VS - GND)$.

It becomes. When a switching circuit switches to the broken-line side of drawing, the partial pressure of this electrical-potential-difference difference is carried out by the capacity factor of capacitors 18 and 19, it becomes electrical-potential-difference between terminals $> (VS - GND)$ of a capacitor 18, and when switches 16 and 17 switch to the continuous-line side of drawing, the charge shown by $C_x \{ \text{electrical-potential-difference between terminals} - (VS - GND) \}$ of a capacitor 18 will be

returned to VS. Relation, such as a ripple, can be explained similarly.

[0075] Namely, this power circuit Input side Electrical potential difference (VS-GND) Current 2I Output side Electrical potential difference $VS'=2x (VS-GND)$ Current Moreover, I can constitute from I the very efficient booster circuit in which both supply and absorption have possible bidirection.

[0076] The effectiveness taken in the example 1 can be acquired by using for the electrical-potential-difference terminal VA of this invention of drawing 1 supply voltage VS' generated by this power circuit. Moreover, although drawing 11 explained making (VS-GND) into twice many electrical-potential-difference [as this] VS', the electrical-potential-difference conversion to integral multiples, such as 3 times and 4 times, is possible by combining more than one further.

[0077] (Example 7) The example when becoming electrical-potential-difference $V0>VA>V2$, and being unable to apply this invention as it is further, in the case of system power circuitry as shown by drawing 3, is shown in drawing 10. Drawing 10 adds the negative electrical-potential-difference generating circuit 15 which generates -VS' ($-VS'<GND$) lower than GND potential by making between VS-GND into supply voltage to drawing 3. Hereafter, if VS is made into the potential of -VS to GND, a detail will be explained about the system in the case of the ability to do lower than the above-mentioned V2 (though natural, when $V3<(GND-VS)=-VS'<V2$ can be satisfied).

[0078] As a negative electrical-potential-difference generating circuit in this case, if it is made the configuration of drawing 12, generating of an electrical potential difference is very efficiently possible. 16 and 17 are equipped with the capacitors 18 and 19 as a transfer switch and a charge storage means in drawing 12. Basic actuation of this circuit is the same as the case of drawing 11. However, since the high-tension side of a capacitor 19 is connected to the terminal of system power GND, it is an output terminal. -VS' will have the electrical potential difference of -VS which turned up VS to the symmetry to GND.

[0079] Therefore, the effectiveness taken in the example 1 can be acquired by using for the electrical-potential-difference terminal VA of this invention of drawing 1 supply voltage-VS' generated by this power circuit. Moreover, although drawing 11 explained making (VS-GND) into a negative electrical potential difference with the potential of -VS, the electrical-potential-difference conversion to integral multiples, such as -2VS and -3VS, is possible by combining more than one further.

[0080] (Example 8) an MOS FET is used for the electrical-potential-difference booster circuit 11 shown in the above-mentioned example 6 as a transfer switch -- very -- a low power -- it is -- power -- it can constitute efficiently. The example of the booster circuit created using the MOS FET is shown in drawing 13. In drawing 13, 20 and 21 are the N-channel metal oxide semiconductor circuits FET, and are illustrated also including internal parasitism diode. Moreover, 22 and 23 are P channel MOS FETs, and are illustrating internal parasitism diode similarly. Furthermore, capacitors 24 and 25 are charge storage means.

[0081] Moreover, the gate voltage clamping circuit of the N-channel metal oxide semiconductor form FET 20, a capacitor 28, and the diode 29 of a capacitor 26 and diode 27 are the gate voltage clamping circuits of P channel MOS FET 22. In addition, the N-channel metal oxide semiconductor form FET 21 "is turned on" on when the gate potential (electrical potential difference between the gate sources) to source potential is more than VS. The N-channel metal oxide semiconductor form FET 20 has the property "is turned on" on when the electrical potential difference between the gate sources is above (forward voltage of VS-diode). Moreover, P channel MOS FET 23 "is turned on" on when the electrical potential difference between the gate sources is below -VS, and P channel MOS FET 22 shall have the property "to turn on", when the electrical potential difference between the gate sources is the following (diode forward voltage-VS).

[0082] Here, ϕ_{iN} which has the amplitude between the electrical potential differences VS and GND as shown in drawing 15 as a gate driving signal, and ϕ_{iP} are inputted. First, T1 period of the gate driving signal of drawing 15 is explained. In T1 period, also in VS level and ϕ_{iP} , ϕ_{iN} serves as VS level, and the N-channel metal oxide semiconductor form FET 21 will be in "ON" condition. Moreover, since the gate of the N-channel metal oxide semiconductor form FET 20 serves as potential of (the forward voltage of the $2xVS$ -diode 27) with a capacitor 26 and diode 27, it will be in "ON" condition. Moreover, ϕ_{iP} is VS level, and by P channel MOS FET 23, source potential and gate potential become the same, and it is set to "OFF." Similarly, with a capacitor 28 and diode 29,

since gate voltage becomes high by the forward voltage of this potential or diode 29 to a source electrical potential difference (a reverse bias is carried out), P channel MOS FET 22 "is turned off" off.

[0083] On the other hand, in T2 period, since ϕ_{IN} serves as GND level also in GND level and ϕ_{IP} , 0V and the electrical potential difference between the gate-sources of the N-channel metal oxide semiconductor form FET 20 serve as the range of $-V_{D27}$ (forward voltage of diode 27) from 0V, and the electrical potential difference between the gate-sources of the N-channel metal oxide semiconductor form FET 21 will both be in an "OFF" condition. Moreover, at P channel MOS FET 23, the electrical potential difference between the GETO sources will be in a next door "ON" condition from VS in the range of $(V_{D29} - V_{D29})$ by VS and P channel MOS FET 22. In addition, in drawing 15, it is creating so that it may have the period all MOS FETs "turn off" off as shown in T12. This is because the N-channel metal oxide semiconductor form 20 and FET 21 and P channel MOS FETs 22 and 23 "are made not to turn on in coincidence."

[0084] As mentioned above, the electrical-potential-difference booster circuit based on the completely same principle of operation as the transfer switch shown by drawing 11 is realizable by operating an MOS FET as a switching device, as shown in drawing 13. In addition, the input impedance of an MOS FET of the gate is very high, and the reason for using an MOS FET as a switching device is that the electrical potential difference between the gate drains at the time of ON is moreover made with about 0. This means that effectiveness for the charge transfer between the capacitors which use the power for driving the gate as that it can do very few and a charge storage means can be made very high. Although a bipolar transistor can naturally be used as a switching device, while needing fixed base current, in a bipolar transistor, the electrical potential difference between collector emitters is not made to below saturation voltage at the time of "ON." Therefore, when this circuit is created using a bipolar transistor, the power conversion effectiveness of a booster circuit is not gathered like an MOS FET.

[0085] Moreover, although the gate drive wave shown in drawing 15 is omitted for details since it can be created simple by the clock generation circuit which uses between VS and GND as a power source, it has the clock for a display in the liquid crystal display, and can create it also by diverting what carried out dividing of this clock.

[0086] (Example 9) an MOS FET is used for the negative electrical-potential-difference generating circuit shown by drawing 12 as a transfer switch -- very -- a low power -- it is -- power -- it can constitute efficiently. The example of the negative electrical-potential-difference generating circuit created using the MOS FET is shown in drawing 14. In drawing 14, 30 and 31 are P channel MOS FETs, and are illustrated also including internal parasitism diode. Moreover, 32 and 33 are the N-channel metal oxide semiconductor forms FET, and are illustrating internal parasitism diode similarly. Furthermore, capacitors 34 and 35 are charge storage means. Moreover, the gate voltage clamping circuit of P channel MOS FET 31, a capacitor 38, and the diode 39 of a capacitor 36 and diode 37 are the gate voltage clamping circuits of the N-channel metal oxide semiconductor form FET 33.

[0087] In addition, the N-channel metal oxide semiconductor form FET 32 "is turned on" on when the gate potential (electrical potential difference between the gate sources) to source potential is more than VS. The N-channel metal oxide semiconductor form FET 33 has the property "is turned on" on when the electrical potential difference between the gate sources is above $(V_{D39} - V_{D39})$ (forward voltage of VS-diode). Moreover, P channel MOS FET 30 "is turned on" on when the electrical potential difference between the gate sources is below $-V_{D30}$, and P channel MOS FET 31 shall have the property "to turn on", when the electrical potential difference between the gate sources is the following $(V_{D37} - V_{D37})$ (diode forward voltage-VS). Here, ϕ_{IN} which has the amplitude between the electrical potential differences VS and GND as shown in drawing 15 as a gate driving signal, and ϕ_{IP} are inputted.

[0088] In T1 period, also in VS level and ϕ_{IP} , ϕ_{IN} serves as VS level, and, in the N-channel metal oxide semiconductor form 32 and FET 33, both the "ON" condition and P channel MOS FETs 30 and 31 of both will be in an "OFF" condition. On the other hand, in T2 period, GND level and ϕ_{IP} are also GND level, and, as for both P channel MOS FETs 30 and 31, are set to "ON", and, as for both the N-channel metal oxide semiconductor forms 32 and FET 33, ϕ_{IN} serves as "OFF." As mentioned above, the negative electrical-potential-difference generating circuit based on the completely same principle of operation as the technique performed by the transfer switch shown by

drawing 12 can be realized by operating an MOS FET as a switching device.

[0089]

[Effect of the Invention] While required components are made into the conventionally same components mark as a circuit by this invention with claim 1 and this equipment according to claim 2 of this invention, it is possible to also lower pressure-proofing of use components. That is, a low power and low cost can be realized.

[0090] when an electrical-potential-difference difference with V2 or V3 electrical potential difference of the supply voltage of system power and liquid crystal driver voltage is small, while being able to acquire the effectiveness taken by claim 1 and claim 2 by having the voltage stabilizer which combined the transistor with claim 3, claim 4, and this equipment according to claim 5 of this invention -- cheap components -- configuration **** -- it also has the cost merit by things.

[0091] With this equipment of this invention according to claim 6, no matter what electrical potential difference system power may have, the effectiveness of low-power-izing as shown in claim 1 can be easily acquired by adding the circuit which carries out the pressure up of the system power electrical potential difference.

[0092] With this equipment of this invention according to claim 7, no matter what electrical potential difference system power may have, the effectiveness of low-power-izing as shown in claim 2 can be easily acquired by adding the circuit which changes system power into a negative electrical potential difference.

[0093] With this equipment of this invention according to claim 8, the booster circuit where power efficiency is moreover well reversible extremely can be created. That is, the liquid crystal driver voltage generator and liquid crystal display which are shown in claim 6 can be efficiently offered by using this booster circuit.

[0094] According to the configuration shown in claim 9, with this equipment of this invention according to claim 9, the negative electrical-potential-difference generating circuit where power efficiency is moreover well reversible extremely can be created. That is, the liquid crystal driver voltage generator and liquid crystal display which are shown in claim 7 can be efficiently offered by using this negative electrical-potential-difference generating circuit.

[Brief Description of the Drawings]

[Drawing 1] It is the circuit diagram showing the driver voltage generator of the liquid crystal display of the basic configuration by this invention.

[Drawing 2] It is the circuit diagram showing the system power of the liquid crystal display applied to the example 1 by this invention.

[Drawing 3] It is the circuit diagram showing the system power of the liquid crystal display applied to the example 2 by this invention.

[Drawing 4] It is drawing having shown the flow of the circuit current by the load of the driver voltage generator of the basic configuration by this invention.

[Drawing 5] It is drawing having shown time amount change of the load which modeled the liquid crystal display of the driver voltage generator of the basic configuration by this invention.

[Drawing 6] It is the circuit diagram showing the driver voltage generator of the liquid crystal display applied to the example 3 by this invention.

[Drawing 7] It is the circuit diagram showing the driver voltage generator of the liquid crystal display applied to the example 4 by this invention.

[Drawing 8] It is the circuit diagram showing the driver voltage generator of the liquid crystal display applied to the example 5 by this invention.

[Drawing 9] It is the circuit diagram showing the system power of the liquid crystal display which added the electrical-potential-difference booster circuit applied to the example 6 by this invention.

[Drawing 10] It is the circuit diagram showing the system power of the liquid crystal display which added the negative electrical-potential-difference generating circuit applied to the example 7 by this invention.

[Drawing 11] It is the circuit diagram showing the basic configuration of the electrical-potential-difference booster circuit of the example 6 by this invention.

[Drawing 12] It is the circuit diagram showing the basic configuration of the negative electrical-potential-difference generating circuit of the example 7 by this invention.

[Drawing 13] It is the circuit diagram showing the electrical-potential-difference booster circuit of the example 8 by this invention.

[Drawing 14] It is the circuit diagram showing the negative electrical-potential-difference generating circuit of the example 9 by this invention.

[Drawing 15] It is the gate drive wave form chart used for the example 8 and example 9 by this invention.

[Drawing 16] It is the approximate account Fig. showing the configuration of the liquid crystal display carried out to this equipment.

[Drawing 17] It is the electrical-potential-difference wave form chart supplied to the common electrode of the liquid crystal display carried out to this equipment.

[Drawing 18] It is the electrical-potential-difference wave form chart supplied to the segment electrode of the liquid crystal display carried out to this equipment.

[Drawing 19] It is drawing having shown the path of a current of flowing with the whole liquid crystal panel of the liquid crystal display carried out to this equipment.

[Drawing 20] It is drawing having shown the flow of the circuit current by the load of the driver voltage generator of the conventional liquid crystal display.

[Description of Notations]

2, 3, 4, 5, 101, 102, 103, 104 Operational amplifier

7, 8, 9 DC to DC converter

10 11, 107, 108 Model load

14 Electrical-Potential-Difference Booster Circuit

15 Negative Electrical-Potential-Difference Generating Circuit

20, 21, 22, 23, 30, 31, 32, 33 MOS FET

51 Driver Voltage Generating Circuit

52 Liquid Crystal Panel

53 Segment Electrode

54 Common Electrode

55 Segment Driver

56 Common Driver